

What is Claimed is:

- 1 1. In a target processor, a trace apparatus
2 comprising:
3 a trigger unit responsive to user and target processor
4 state input signals, the trigger unit generating control
5 signals in response to the input signals;
6 timing trace apparatus, the timing trace apparatus
7 responsive to control signals for selectively providing
8 timing trace streams during secondary code execution;
9 program counter/data trace apparatus, the program
10 counter/data trace apparatus responsive to signals from the
11 control apparatus for selectively providing program
12 counter/data trace streams during secondary code execution
13 when the timing trace unit is providing signal during the
14 secondary code execution.
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- 16 2. The trace apparatus as recited in claim 1 wherein
17 secondary code execution is background/interrupt service
18 routine code execution.
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- 20 3. The trace apparatus as recited in claim 1 wherein
21 the target processor is can have one of an unprotected
22 pipeline and a protected pipeline.
23
- 24 4. The trace apparatus as recited in claim 1 further
25 comprising a pipeline flattener, the pipeline flattener

1 aligning the program counter address with the completion of
2 the instruction, the pipeline flattener flushing
3 instructions in response to a halt execution signal in an
4 unprotected pipeline, the pipeline flattener halting
5 operation in a protected pipeline.

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7 5. The trace apparatus as recited in claim 1 where
8 in the target processor has three states, a primary code
9 execution state, a secondary code execution state, and an
10 execution halt state.

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12 6. The trace apparatus as recited in claim 5 wherein
13 the timing trace stream can be controllably enabled during
14 an execution halt state.

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16 7. A method of controlling trace streams in a target
17 processor, the method comprising:

18 generating a timing trace stream in the target
19 processor in response to preselected user and target
20 processor input signals; and

21 when the timing trace stream is being generated,
22 generating a program counter and a data trace stream in
23 response to predetermined user and target processor input
24 signals.

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26 8. The method as recited in claim 7 further
27 comprising including in the target processor input signals

1 indicia of the state of the target processor, the target
2 processor having a primary code execution state, a
3 secondary code execution state and an execution halt state.

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5 9. The method as recited in claim 7 further
6 comprising including in the target processor input signals
7 indicia indicating whether the target processor was in a
8 protected pipeline mode of operation or in an unprotected
9 pipeline mode of operation.

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11 10. The method as recited in claim 7 further
12 comprising including in the user input signals whether the
13 timing trace was enabled during instruction execution
14 halts.

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16 11. The method as recited in claim 9 further
17 comprising including in the user input signals whether the
18 timing trace stream was enabled during the secondary code
19 execution state.

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21 12. A processing unit comprising:

22 a central processing unit, the central processing unit
23 having three states of operation, a primary code execution
24 state, a secondary code execution state and an execution
25 halted state; and

26 trace generating apparatus including

1 program counter generation and a data trace
2 stream generation unit, the program counter trace stream
3 generation unit and the data trace generation unit
4 responsive to control signals for generating the program
5 counter and the data trace streams respectively;

6 a timing trace stream generation unit, the timing
7 trace stream generation unit generating a timing trace
8 stream in response to control signals; and

9 a trigger unit responsive to user input signals
10 and to central processing unit signals for generating
11 control signals controlling the timing trace generation
12 unit and the program counter and data trace generation
13 unit.

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15 13. The processing unit as recited in claim 12
16 wherein first control signals enable the timing trace
17 generation unit during the secondary code execution state.

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19 14. The processing unit as recited in claim 13
20 wherein second control signals enable the timing trace
21 generation device and the program counter and data trace
22 generation units during the secondary code execution.

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24 15. The processing unit as recited in claim 12
25 including indicia of a protected pipeline mode of operation
26 and of an unprotected mode of operation of the central

1 processing unit are part of the central processing unit
2 input signals.
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